COMPRESSIVE (PFET) AND TENSILE (NFET) CHANNEL STRAIN IN NANOWIRE FETS FABRICATED WITH A REPLACEMENT GATE PROCESS

FIELD OF THE INVENTION

The present invention relates to semiconductor-based electronic devices, and more particularly, to field-effect transistor (FET) devices having nanowire channels and techniques for fabrication thereof.

BACKGROUND OF THE INVENTION

With nanowire-based field effect transistors (FETs), the nanowires serve as channels of the device interconnecting a source region and a drain region. A gate surrounding the nanowire regulates electron flow through the channels. When the gate completely surrounds a portion of each of the nanowire channels, this configuration is referred to as a gate-all-around (GAA) device. GAA nanowire-based FETs have excellent scaling properties and are presently investigated as building blocks for future complementary metal-oxide semiconductor (CMOS) technology.

Process-induced channel strain is presently used to enhance device performance. Namely, compressive strain is used with p-channel FETs (PFETs) to improve the hole mobility and tensile strain is used with n-channel FETs (NFETs) to improve the electron mobility. While the techniques for inducing channel strain in planar CMOS devices are relatively straightforward, this is not the case with nanowire-based devices. Applying channel strain in the case of nanowire FETs is challenging.

Therefore, process-induced channel strain techniques for GAA nanowire-based FETs would be desirable.

SUMMARY OF THE INVENTION

The present invention provides field-effect transistor (FET) devices having nanowire channels and techniques for fabrication thereof. In one aspect of the invention, a method of fabricating a FET device is provided. The method includes the following steps. Nanowires and pads are formed in a silicon-on-insulator (SOI) layer over a buried oxide (BOX) layer, wherein the nanowires are connected to the pads in a ladder-like configuration, and wherein the nanowires are suspended over the BOX. A hydrogen silsesquioxane (HSQ) layer is deposited that surrounds the nanowires. One or more portions of the HSQ layer that surround the nanowires are cross-linked, wherein the cross-linking causes the one or more portions of the HSQ layer to shrink thereby inducing strain in the nanowires. One or more gates surrounding portions of each of the nanowires are formed, wherein the gates retain the strain induced in the nanowires by the cross-linking step, and wherein the portions of the nanowires surrounded by the gates comprise channel regions of the device and portions of the nanowires extending out from the gates and the pads comprise source and drain regions of the device.

In another aspect of the invention, a FET device is provided. The FET device includes nanowires and pads formed in a SOI layer over a BOX layer, wherein the nanowires are connected to the pads in a ladder-like configuration, and wherein the nanowires are suspended over the BOX; one or more gates surrounding portions of each of the nanowires, wherein the portions of the nanowires surrounded by the gates comprise channel regions of the device and portions of the nanowires extending out from the gates and the pads comprise source and drain regions of the device; wherein each of the nanowires has 1) at least one first region that is deformed such that a lattice constant in the at least one first region is less than a relaxed lattice constant of the nanowires and 2) at least one second region that is deformed such that a lattice constant in the at least one second region is greater than the relaxed lattice constant of the nanowires, and wherein the one or more gates surround either the at least one first region or the at least one second region of each of the nanowires. A more complete understanding of the present invention, as well as further features and advantages of the present invention, will be obtained by reference to the following detailed description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A is a cross-sectional diagram illustrating a starting structure for a field-effect transistor (FET) device fabrication process, i.e., a plurality of nanowires and pads formed in a silicon-on-insulator (SOI) layer, wherein the nanowires have been thinned/reshaped and are suspended over a buried oxide (BOX) according to an embodiment of the present invention;

FIG. **1**B is a top-down diagram of the structure of FIG. **1**A which shows that the nanowires and pads are formed in a ladder-like configuration wherein the nanowires connect the pads like rungs of a ladder according to an embodiment of the present invention;

FIG. **2**A is a cross-sectional diagram illustrating a hydrogen silsesquioxane (HSQ) layer having been deposited so as to surround the suspended nanowires and the HSQ having been patterned by cross-linking which causes the patterned HSQ to shrink thereby inducing strain in the nanowires according to an embodiment of the present invention;

FIG. **2**B is a top-down diagram of the structure of FIG. **2**A which illustrates the patterned HSQ surrounding the nanowires, wherein the patterned HSQ serves as dummy gates in the fabrication process according to an embodiment of the present invention;

FIG. **3** is a cross-sectional diagram illustrating spacers having been formed adjacent to sidewalls of the patterned HSQ dummy gates and a filler material having been deposited onto the structure, surrounding exposed portions of the nanowires according to an embodiment of the present invention;

FIG. **4** is a cross-sectional diagram illustrating the patterned HSQ dummy gates having been replaced with a gate conductor to form replacement gates according to an embodiment of the present invention;

FIG. **5** is a cross-sectional diagram illustrating the filler material having been removed and an epitaxial film having been formed on the nanowires and pads according to an embodiment of the present invention;

FIG. **6** is a cross-sectional diagram illustrating final processing steps being performed to complete the device, including forming form source/drain contacts according to an embodiment of the present invention;

FIG. **7**A is a cross-sectional diagram illustrating an HSQ layer surrounding suspended nanowires prior to cross-linking and annealing according to an embodiment of the present invention;

FIG. **7**B is a cross-sectional diagram illustrating the strain induced in the nanowires of FIG. **7**A after the HSQ has been cross-linked and annealed according to an embodiment of the present invention;

FIG. **8** is a cross-sectional diagram illustrating in an alternative process (following from FIG. **1**A) an HSQ layer having been deposited so as to surround the suspended nanowires